I/O System views

Note Title 12/3/2008

Proj. 4 Combining Functions

IMPL

AND

S	D	Res
0	0	0
0	1	0
1	0	0
1	1	1

Project Due: midnight - 11:59PM Friday.

(1)

Protection of I/O resources:

I/O devices are "owned" by the O.S.

- Some things are not allowed to be done by user programs.
  - for memory mapped I/O
    - Protection using page tables

Processor modes: user — unprivileged
kernel — privileged.

on intel processors — modes to implement completely different instruction sets.

DMA

(2) Direct Memory Access I/O

Multi-word transfers w/o assistance from CPU:

DMA controller that is given a command

move n bytes from this device to this address

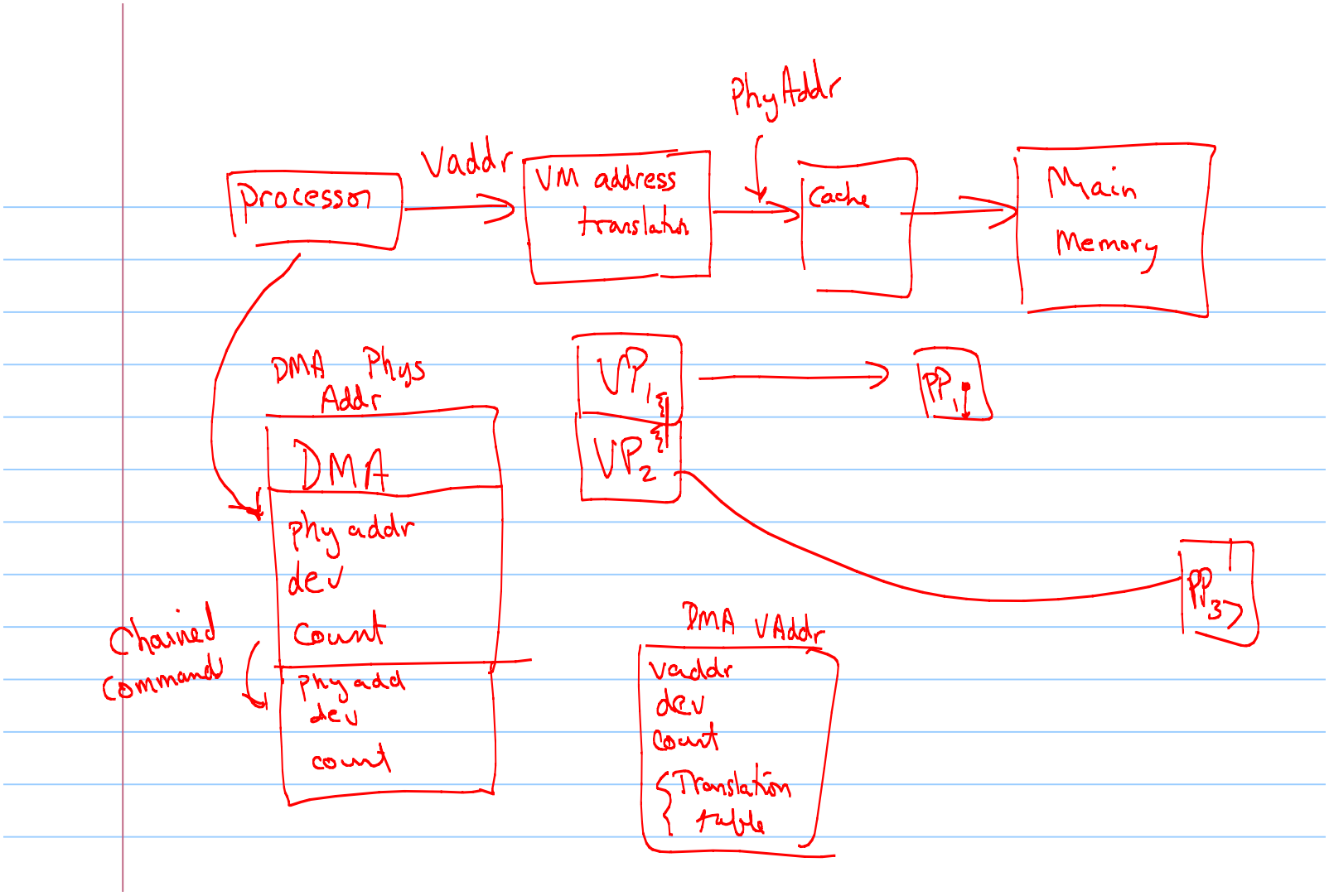
when finished cause an interrupt

Issues:

It's not free.

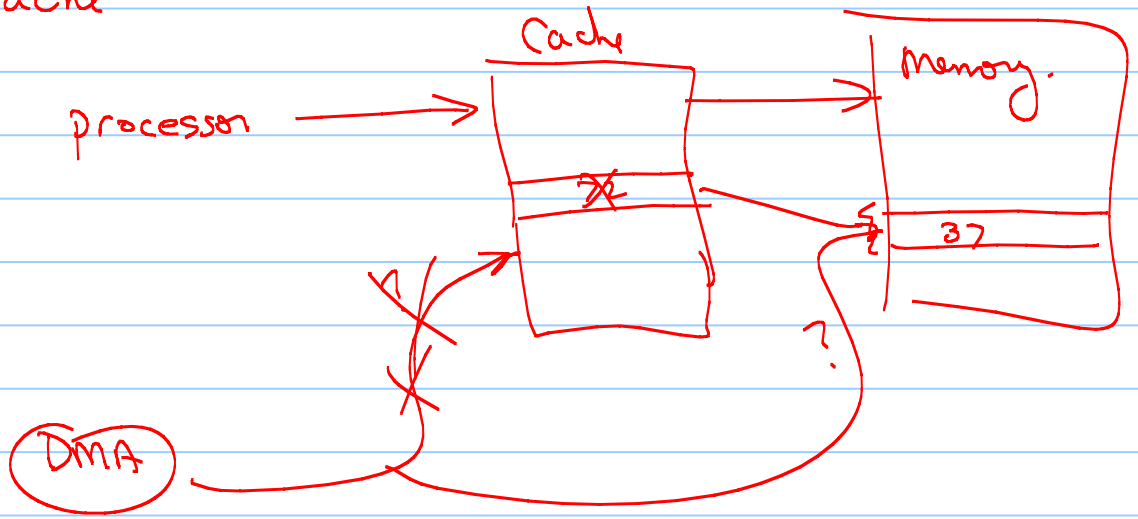
DMA is using the memory system — processor may have to wait due to interference from DMA.

What are the interactions w/ VM and caches?


Processor
Vaddr
VM address translation
PhyAddr
Cache
Main Memory
DMA Phys Addr
DMA
phy addr
dev
Count
Chained Commands
Phy add
dev
count
VP1
VP2
PP1
PP3
DMA VAddr
vaddr
dev
Count
Translation table

2b

Cache



DMA read — read from device
write into memory

DMA not into cache requires Cache invalidation mechanism.